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US Army Research Laboratory

Effects of Growth Conditions on the Measured Electrical Properties of Monolayer Molybdenum Disulfide

by Alexander L Mazzoni, Robert A Burke, Matthew L Chin, and Matthew J Hwee

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14. ABSTRACT
Molybdenum disulfide (MoS_2) is a 2-D material that shows promise for flexible electronics, low-power applications, and optoelectronics due to its atomic thickness, high strain limit, large I_{on}/I_{off}, and direct bandgap. We report on the electrical characterization of MoS_2 transistors fabricated from US Army Research Laboratory-grown MoS_2 and focus on how the MoS_2 growth conditions affect the electrical performance. Metrics such as electron mobility, threshold voltage, hysteresis, and contact resistance are calculated for multiple devices on each growth condition. Measured devices had an electron mobility in the range of 1–15 $cm^2/V{\cdot}s$. MoS_2 grown with lower sulfur precursor purity had the lowest mobility and a negatively shifted threshold voltage. A longer MoS_2 growth time led to devices with the highest measured mobility. Transferring the MoS_2 to a new substrate and modifying the growth setup to a 2-boat process show potential for improving device performance and prompt further investigation.

15. SUBJECT TERMS
2-D materials, molybdenum disulfide, MoS_2, field-effect transistor, electron mobility, powder vaporization

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1. Introduction

Starting with the isolation of graphene from a bulk graphite crystal in 2004,[1] research in 2-D materials has exploded over the last decade.[2] One of the major limitations of graphene is the fact that it does not possess a bandgap. As a result, a variety of 2-D materials have been exfoliated, synthesized, or proposed to find a suitable alternative beyond graphene for applications such as digital and low-power electronics where a bandgap is necessary. Perhaps the most popular of these alternative materials is molybdenum disulfide (MoS_2), a semiconducting member of the transition metal dichalcogenide family.

Initial studies involving MoS_2 used flakes that were exfoliated from bulk MoS_2 crystals,[3] akin to initial graphene studies. The last few years have seen an increase in the capability and quality of large-area MoS_2 growth, with powder vaporization (PV)[4,5] and chemical vapor deposition (CVD)[6] being the most common growth methods.

At the US Army Research Laboratory, MoS_2 is synthesized on a silicon dioxide (SiO_2) substrate via atmospheric pressure PV using sulfur (S) and molybdenum trioxide (MoO_3) powder precursors. In this growth system, variables such as substrate preparation, precursor temperature and location, substrate/growth temperature, system configuration, and growth time are explored to investigate their impact on the properties of MoS_2. In this study, we investigate the impact of the growth conditions on the electrical properties of MoS_2. Electron beam lithography (EBL) is used to fabricate field-effect transistors (FETs) from single-crystal, monolayer MoS_2 triangles. Important device properties such as carrier mobility, sheet resistance, and contact resistance are extracted from the FETs. Several devices are fabricated on each set of growth conditions to elucidate any correlation between the growth parameters and the resulting electrical properties.

2. Methods

2.1 Growth

Prior to growth, highly doped (p++) silicon (Si) substrates with a 220-nm thermal oxide were soaked in piranha etch (3:1 ratio of sulfuric acid [H_2SO_4]:hydrogen peroxide [H_2O_2]) for 15 min, followed by 5-min soaks in deionized (DI) water, acetone, and isopropyl alcohol (IPA). The samples were rinsed with DI water and dried with nitrogen. Afterward, the substrates were treated in an oxygen plasma for 5 min to create a hydrophilic surface, and then perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS) was spin coated onto the samples at 500 rpm for

5 s, 2,000 rpm for 45 s, and then 4,000 rpm for 15 s to prevent excess PTAS in the corners of the sample. The spun PTAS is an incomplete film and acts as a seeding layer for growth. Two different growth setups were used for this study, named for the number of boats used to hold the samples and precursors. The primary setup for these experiments was the 3-boat configuration. For the 3-boat setup, substrate size was 9 mm × 9 mm and used 20 µL of PTAS solution. The 2-boat setup used 15 mm × 17 mm substrates and 40 µL of PTAS solution.

2.1.1 3-Boat Growth Setup

Four samples (9 mm × 9 mm) were placed face up in an alumina crucible (CoorsTek) and loaded into the center of a tube furnace (Fig. 1). MoO_3 powder (Sigma Aldrich, 99.5%) was added to a second alumina boat and loaded next to the samples, while sulfur powder (Sigma Aldrich, 99.98%) was added to a third alumina boat and loaded upstream of the MoO_3 powder and substrates. The system was sealed and purged with 200 sccm of argon for 10 min. Afterward, the argon flow rate was reduced to 5 sccm and the tube furnace was heated at a rate of approximately 17 °C/min until it reached its growth temperature. The temperature set point of the heating tape for the sulfur source was set (normally to 250 °C) 3 min before the system reached growth temperature (normally 700 °C). Once the growth step was complete (typically 10 min), the heating tape was turned off, the furnace was opened, and the argon flow rate was increased to 200 sccm to quench the growth process. The system was cooled for 25–30 min before unloading the samples from the furnace.

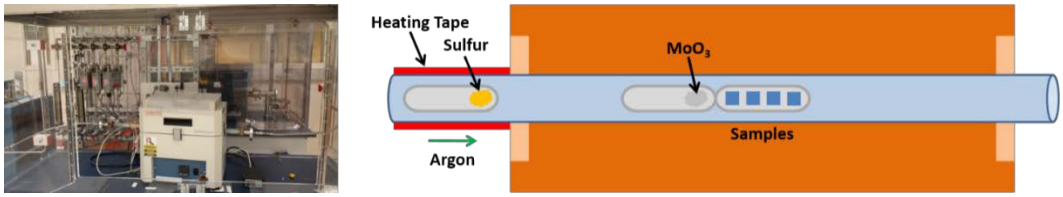

Fig. 1 Picture (left) and diagram (right) of the MoS_2 PV system. The system consists of a tube furnace and heating tape. Alumina boats were used for holding the MoO_3 powder, sulfur powder, and the substrates for growth. The substrates were placed face up in the alumina boat. Argon was used as a carrier gas for the growth process.

2.1.2 2-Boat Growth Setup

The boat configuration was modified to a 2-boat setup in an attempt to improve the quality of the MoS_2 growth. In this configuration, the MoO_3 powder and the substrates were loaded in the same alumina boat. Four samples (15 mm × 17 mm) were placed across the top of the alumina boat (face up for individual triangle domains and face down for continuous monolayer growth). The MoO_3 powder was spread along the base of the alumina boat. A diagram of the 2-boat setup is shown in Fig. 2. All other parts of the growth process are identical to the 3-boat process.

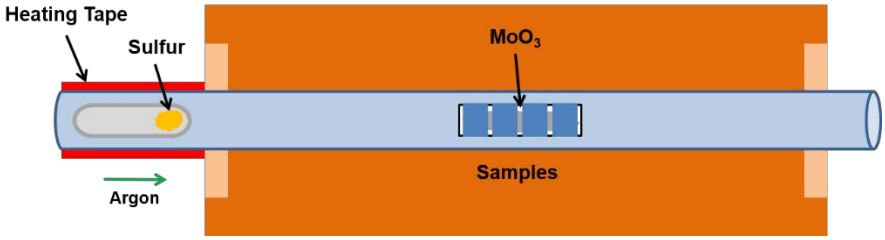

Fig. 2 Diagram of the modified MoS_2 PV system. In this configuration, the MoO_3 powder and the substrates were loaded in the same alumina boat. The samples were placed on top of the alumina boat (face up for individual triangle domains and face down for continuous monolayer growth). The MoO_3 powder was spread along the base of the alumina boat.

2.1.3 Growth Conditions

Using the growth setup described previously, we investigated the effect of the growth conditions on the electrical properties of monolayer MoS_2. Variables that we explored included growth temperature (650–700 °C), sulfur temperature (200–250 °C), and sulfur precursor purity (≥99.98% and ≥95%). Based on the optical microscopy results, device fabrication was carried out on samples where triangular MoS_2 growth was observed. Details for the growths used for device fabrication and electrical testing are provided in Table 1.

Table 1 Table of the growth conditions used for each device set

Sample ID	Growth temp (°C)	Sulfur temp (°C)	Boat setup	Growth time (min)
APM077C[1]	700	250	3-boat	10
APM089C	700	250	3-boat	50
APM103A[1]	700	250	3-boat	10
APM104C[2]	700	250	3-boat	10
APM106A	700	200	3-boat	10
APM108A	650	250	3-boat	10
APM198A[3]	700	250	3-boat (transferred)	10
APM198B[3]	700	250	3-boat (as-grown)	10
APM211B	700	250	2-boat, face up	10

[1]Grown using the same conditions (testing reproducibility).
[2]Grown using a lower purity sulfur (≥95% vs. ≥99.98%).
[3]Same growth conditions, but 198A was transferred via potassium hydroxide (KOH) etching to a new SiO_2 substrate.

Samples 77C and 103A were grown using the same conditions to test reproducibility. In an attempt to grow a continuous monolayer, the growth time was increased from 10 to 50 min for 89C. Optical microscope images of samples that were used for electrical characterization are provided in Fig. 3.

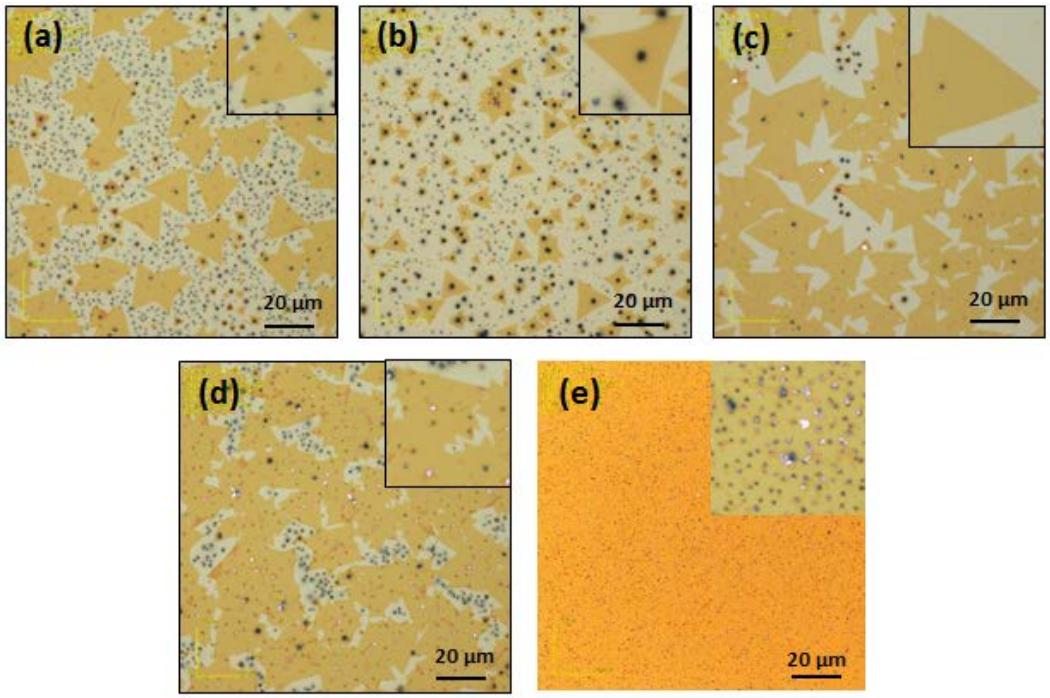

Fig. 3 Representative optical microscope images of different MoS_2 growths: MoS_2 triangles grown on SiO_2/Si a) using our standard conditions (77C, 103A, 198B), b) at a sulfur temperature of 200 °C (106A), c) at a furnace temperature of 650 °C (108A), d) using a lower purity (≥95%) sulfur powder (104C), and e) continuous monolayer MoS_2 film as a result of a longer growth time (89C)

2.2 Device Fabrication

Due to the length of the growth step, typically an incomplete film with individual, triangular MoS_2 domains was formed on the SiO_2 surface. Additionally, the growth had areas of multilayer MoS_2 and particle contamination (mostly MoS_2 with some molybdenum oxysulfide [MoO_xS_y]). As a result, it was necessary to develop a process to target the individual monolayer MoS_2 triangles (varying in size from 5 to 50 µm depending on the growth condition) for device fabrication. The following sections describe the process flow for device fabrication of the as-grown material on the original substrate and also after transfer of the MoS_2 material to a new substrate.

2.2.1 Process Flow

All patterning for deposition and etching steps was achieved through standard EBL techniques using a 950 poly(methyl methacrylate) (PMMA) A4 resist (MicroChem). The PMMA was spin coated at 2,000 rpm (thickness around 300 nm) and then baked on a hotplate at 185 °C for 2 min. The PMMA was exposed using a proximity effect correction with a base dose of 850 μC/cm^2. Development of the PMMA was performed using a 10-mL:25-mL methyl isobutyl ketone (MIBK):IPA solution for 75 s with manual agitation.

A titanium/gold (Ti/Au) marker layer (10 nm Ti /90 nm Au) in the shape of a coordinate grid was first deposited via electron beam evaporation (CHA Industries) and liftoff in acetone. This marker layer helped to determine clean, monolayer MoS_2 locations for device fabrication and also served as an alignment layer during the EBL process for the following steps (Fig. 4).

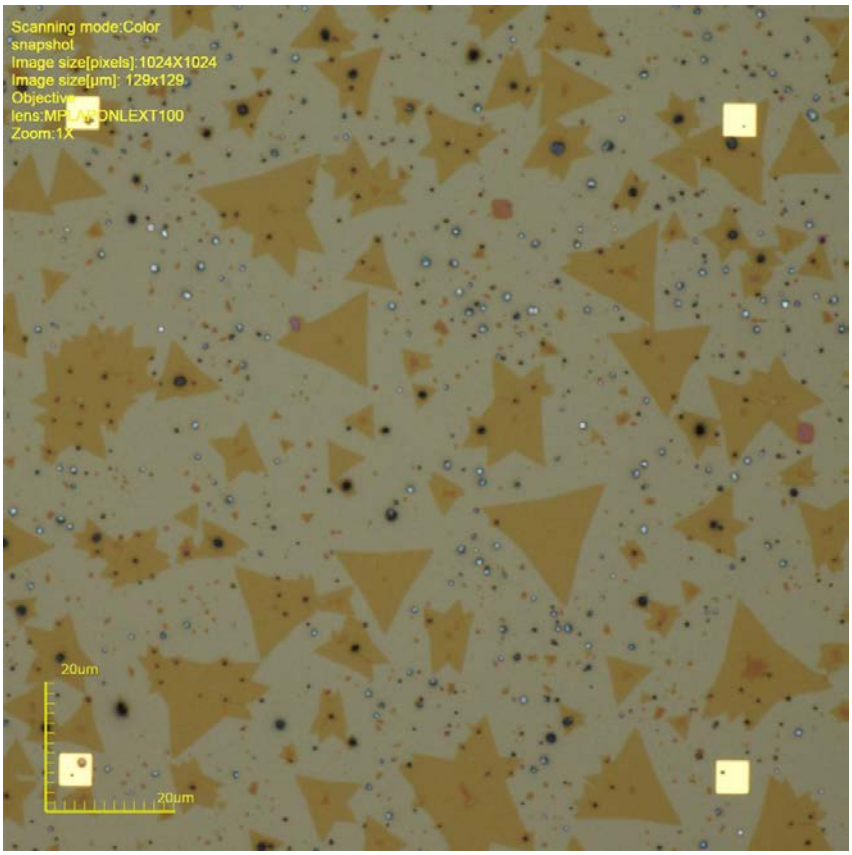

Fig. 4 Optical microscope image of a 100-μm × 100-μm region of MoS_2 grown on 220 nm of SiO_2 after marker layer deposition and liftoff. The yellow-orange triangular structures are monolayer domains of MoS_2 and are the areas that were targeted for device fabrication. Darker orange areas in the center of the MoS_2 triangles are areas of bilayer to few-layer growth and were avoided during device fabrication. The 4 squares are part of the metal marker coordinate grid deposited over the entire sample.

Next, using a PMMA etch mask (Fig. 5), the MoS_2 channel dimensions were formed through 45 s of reactive ion etching (RIE) using 15 sccm of tetrafluoromethane (CF_4), 5 sccm of oxygen (O_2), and 200 W of radio frequency (RF) power (Ulvac NE550e Etcher).

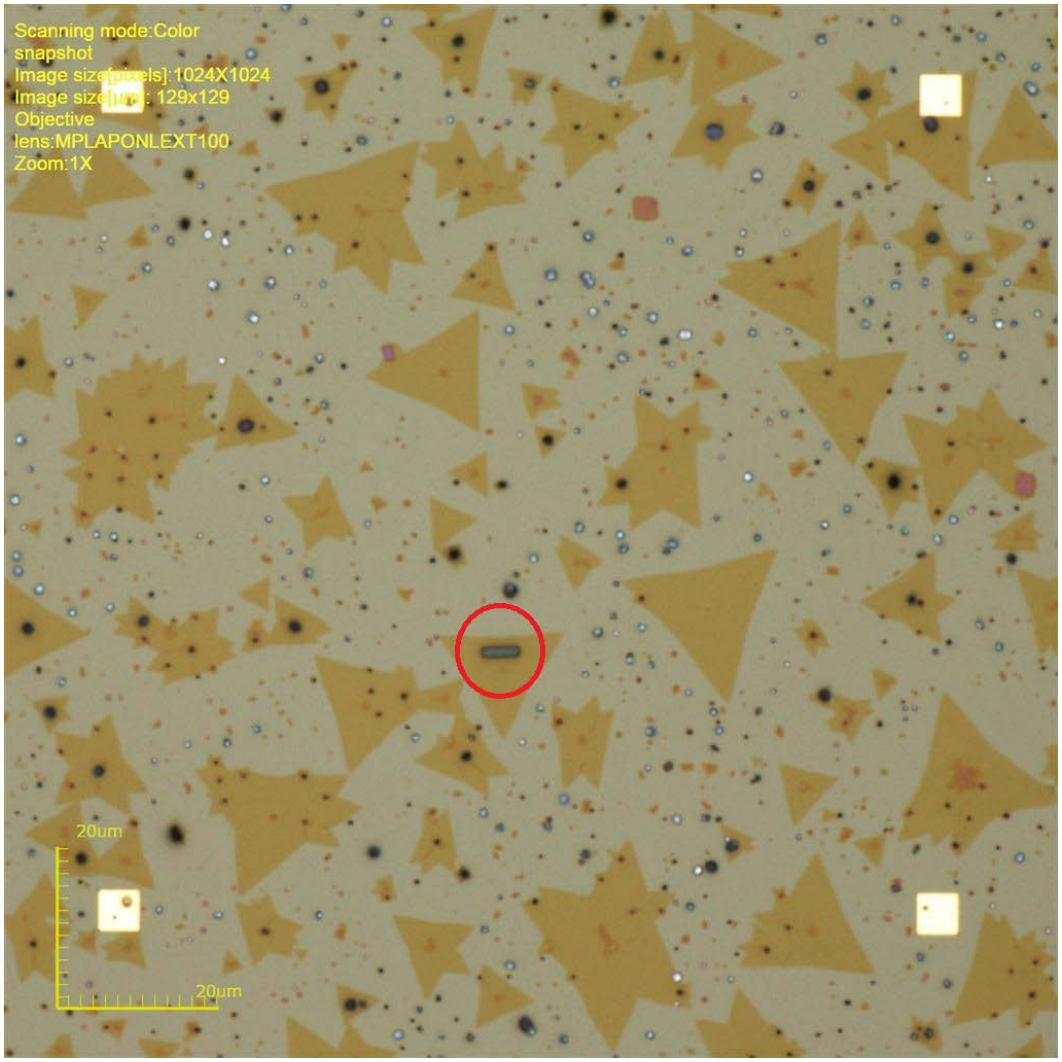

Fig. 5 Optical microscope image of the same area as Fig. 4, after the channel-defining EBL. The bar inside the circled region is PMMA that protects the area of MoS_2 below it during the subsequent RIE. All other areas of MoS_2 need to be removed to prevent unintentional conduction pathways between the measurement probes.

After etching, the PMMA was removed by an acetone bath. Ti/Au contacts (10 nm/90 nm) to the MoS_2 monolayer were deposited (Fig. 6) via electron beam evaporation (Evatec BAK 641) at a pressure less than 1×10^{-6} Torr, followed by liftoff of the excess metal in an acetone bath.

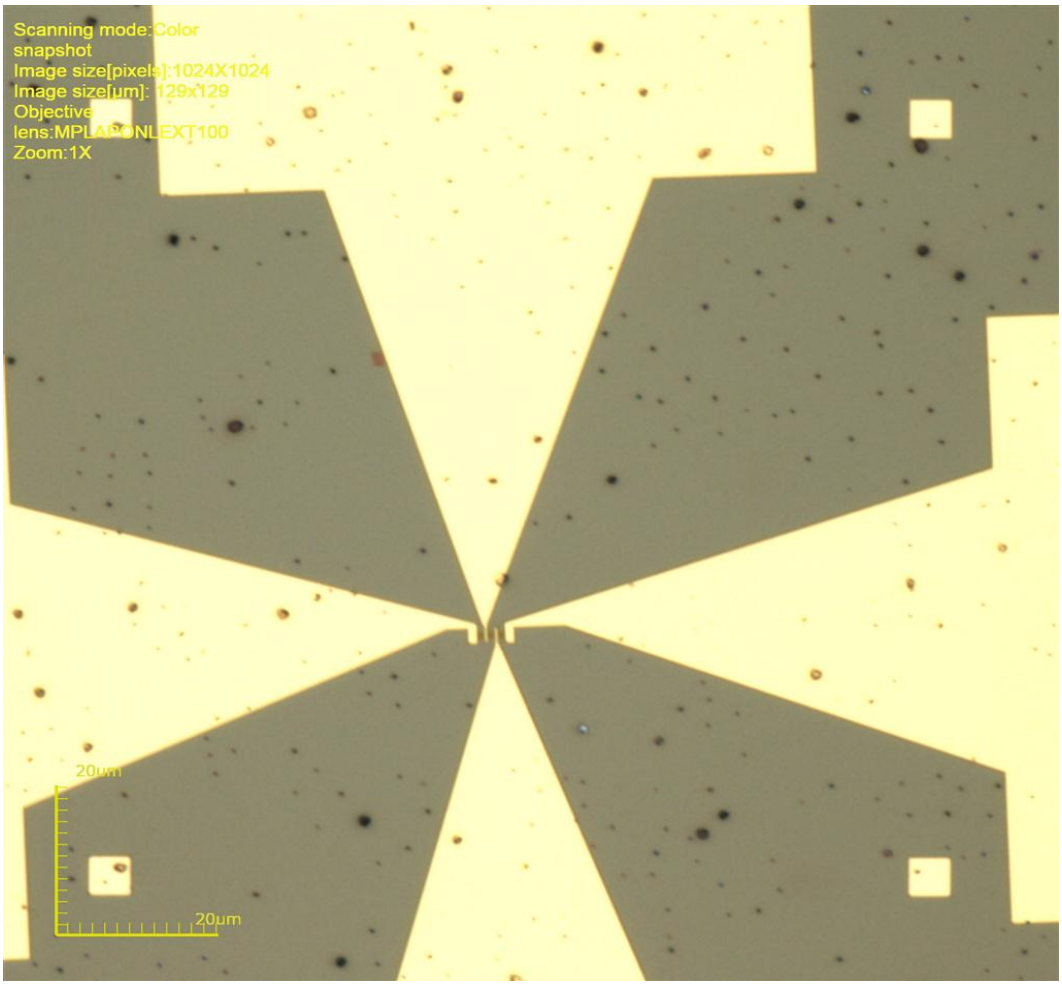

Fig. 6 Optical microscope image of the same area as Figs. 4 and 5, after the MoS_2 etch and metal contact deposition

A cross-sectional view of the final device structure is shown in Fig. 7. The highly p-doped Si wafer acts as a global back gate electrode and the 220 nm of SiO_2 is the gate dielectric.

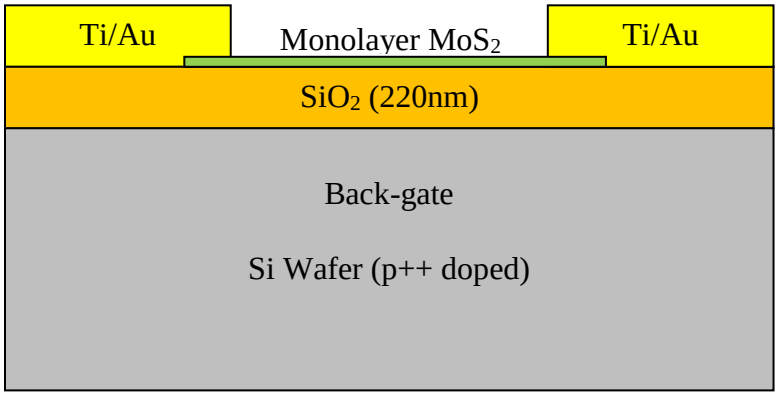

Fig. 7 Cross-sectional drawing of the back-gated MoS_2 FET structure

The samples were batch-processed as often as possible (e.g., metal evaporation, etching, and cleaning) to limit differences in the electrical properties resulting from inconsistencies in the fabrication process between the samples. Samples 77C, 89C, 104C, 106A, 108A, and 198B were fabricated together; 211B, 198A, and 103A were fabricated together at a later date. The exact same fabrication processes were used for both sets of samples. Samples were also kept in a nitrogen atmosphere prior to device fabrication to help prevent material degradation.[7]

2.2.2 MoS_2 Material Transfer

In this study, every device set except for one was fabricated out of "as-grown" MoS_2 on SiO_2. For the unique sample (APM198A), the MoS_2 was transferred from the SiO_2 growth substrate to a new SiO_2 substrate. The transfer process used a PMMA spin-cast layer to protect the MoS_2 and potassium hydroxide (KOH) to separate the MoS_2 from the SiO_2 growth substrate. The transfer process can potentially improve performance by relaxing growth-induced strain and removing interfacial impurities from the growth process.[8] However, the transfer process can also lead to wrinkling of the MoS_2 and leave PMMA residue.[9] The transfer process is also known to degrade performance in graphene devices via residual resist, metallic impurities, or interfacial water.[10]

The specific details for the transfer process are as follows.

PMMA 950 A9 was spun onto the $MoS_2/SiO_2/Si$ stack at 2,000 RPM for 60 s and then soft baked at 50 °C in air for 30 min. After air-drying in a fume hood for an additional 3 h at room temperature, the PMMA was scraped from the edges of the growth substrate with a razor blade.

A solution of 15% KOH by weight was prepared by dissolving KOH pellets in DI water. The PMMA-coated MoS_2 substrate was floated on the KOH solution at room temperature and left in the solution until interfacial interactions between the MoS_2, SiO_2, and KOH solution caused the $PMMA/MoS_2$ layer to release from the SiO_2/Si substrate.

Upon release, the MoS_2 with the PMMA handling layer was transferred from the KOH solution into a DI water bath, where it was floated for 10 min to disperse any KOH residue still present on the MoS_2. This $PMMA/MoS_2$ film stack was transferred again to another DI water bath, where it sat for another 10 min to further dilute any KOH residue. Finally, the $PMMA/MoS_2$ film stack was transferred onto the target substrate within the DI water bath. The target substrate was composed of a Si substrate with 220 nm of thermally grown SiO_2 and a Ti/Au marker layer deposited on top. Once the transfer was complete, the $PMMA/MoS_2$ film stack was

lightly dried with nitrogen gas (N_2) to remove any interfacial water. The sample was then dried at room temperature in a fume hood overnight.

After drying overnight, the PMMA layer was removed from the MoS_2 by immersing the sample in an acetone bath heated to 60 °C for 30 min followed by an additional 2-h acetone soak at room temperature. Afterwards, the sample was taken out of the acetone, rinsed with IPA, dried using N_2, and loaded into an annealing furnace to remove any remaining PMMA residue. Then, 200 sccm of forming gas (4.5% hydrogen, 95% argon) was flown over the substrate for 1 h at a temperature of 250 °C, at which point, the annealing furnace was allowed to cool to room temperature. At this point, the transferred MoS_2 film was ready for processing.

2.3 Electrical Characterization

2.3.1 Device Dimensions

The same device structure was created on every MoS_2 sample to provide a direct comparison of electrical performance. The device created was a FET in a 4-point probe (4PP) configuration. A drawing of the device used, including dimensions and probe testing configuration, is shown in Fig. 8.

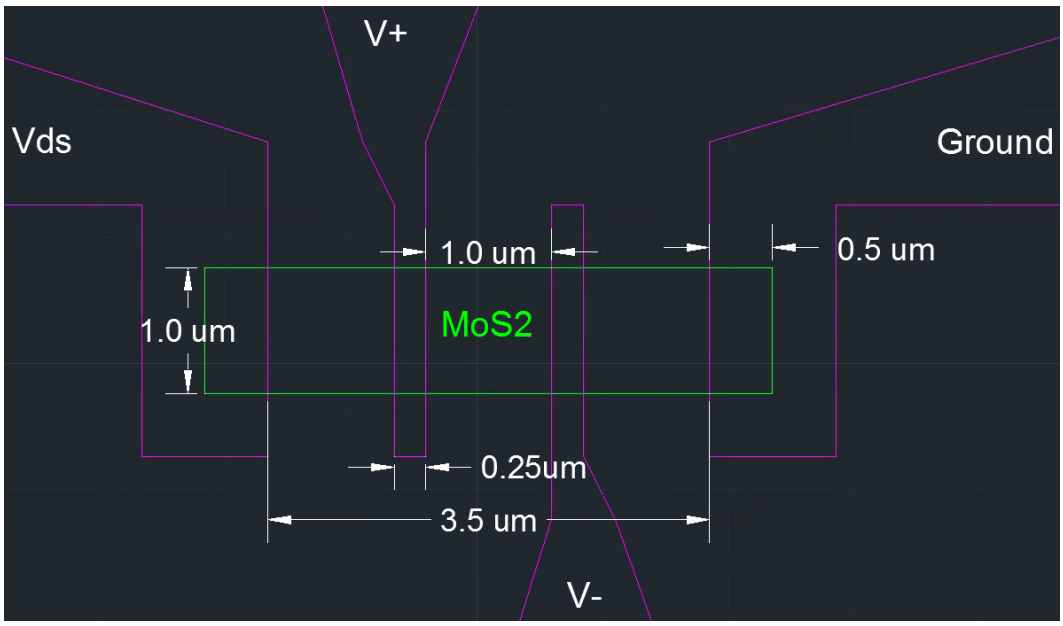

Fig. 8 Top-down drawing of the computer-aided design used to create the MoS_2 FET. The green rectangle represents the area of monolayer MoS_2 and purple represents the areas of the Ti/Au metal contacts.

For the electrical characterization of this device, the following variables and constants are introduced:

- $R_{2PP} = V_{ds}/I_{ds}$ is the resistance measured between the outer 2 probes.
- $V_{diff} = V^+ - V^-$ is the voltage difference measured between the inner 2 probes.
- $R_{4PP} = V_{diff}/I_{ds}$ is the resistance measured between the inner probes.
- $\frac{L}{W_{4PP}} = 1$ is the length over width ratio of the MoS_2 channel between the inner probes.
- $\frac{L}{W_{2PP}} = 3.5$ is the length over width ratio of the MoS_2 channel between the outer probes.

2.3.2 Testing Procedure/Conditions

All devices were tested at room temperature in a vacuum probe station at a pressure no higher than 5×10^{-6} Torr. Prior to testing, the devices were annealed overnight at 400 K in vacuum. A Keithley 4200 Semiconductor Characterization System was used to perform the electrical measurements. The viewport was covered with aluminum foil to block any light from entering the probe station and ensure no impact from photosensitivity (sensitivity to light was observed, but not characterized; the Appendix shows examples of the photosensitivity measured). Devices were tested with a constant drain-source bias (V_{ds}) of 100 mV, while sweeping the back-gate voltage (V_{bg}) back and forth from –30 to +60 V. A typical transfer curve obtained with this procedure is shown in Fig. 9. This transfer curve example is used in the following sections to illustrate how the device performance metrics were extracted.

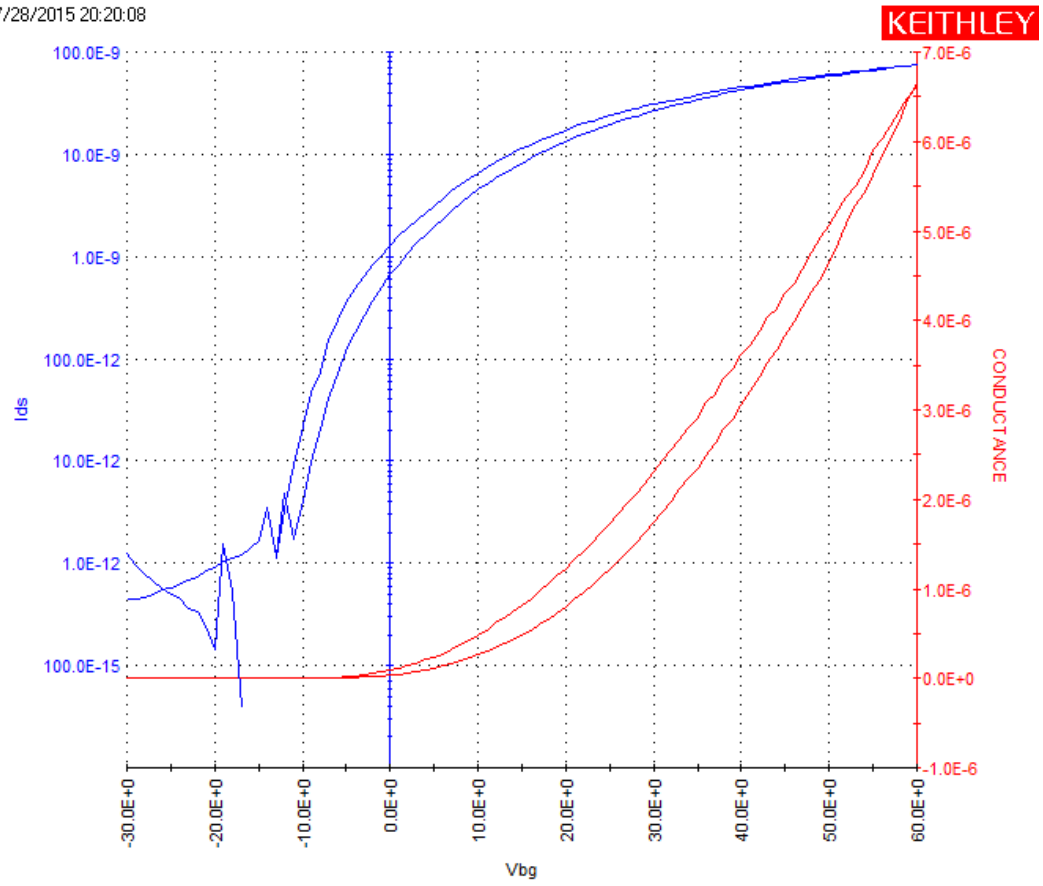

Fig. 9 Example device (F2 of 77C) data obtained with the testing conditions described previously. The blue curve plots (log scale) the current flowing in the transistor and the red curve plots (linear scale) the conductance measured as I_{ds}/V_{diff}.

Similar to the fabrication methods, devices were batch-tested in the probe station to limit the possibility of the device performance differing because of variations in the testing environment.[11] The samples were tested in 2 groups based on which fabrication iteration they were a part of. Samples 77C, 89C, 104C, 106A, 108A, and 198B were tested in the first group. Samples 211B, 198A, and 103A were tested in the second group. It should be noted that the first batch of samples were annealed under vacuum twice as a broken probe (requiring venting of the probe station chamber to fix) prevented testing after the initial anneal.

2.3.3 Sheet Resistance Extraction

Sheet resistance, R_{sh}, is often used to describe the electrical properties of 2-D materials as it removes the geometrical dependence a pure resistance value has and does not require knowledge of the thickness, which is needed for calculating the resistivity. Using the previously defined constants, the equation for the sheet resistance is

$$R_{sh} = \frac{R_{4PP}}{\frac{L}{W_{4PP}}} \quad [\Omega/\square]. \tag{1}$$

For this particular device design, the MoS_2 channel between the inner voltage sensing probes has a length and width of 1 μm, meaning the sheet resistance is the same as R_{4PP}. Figure 10 shows the measured 4PP resistance (sheet resistance) and 2-point probe (2PP) resistance for the example device over the entire range of back-gate voltages.

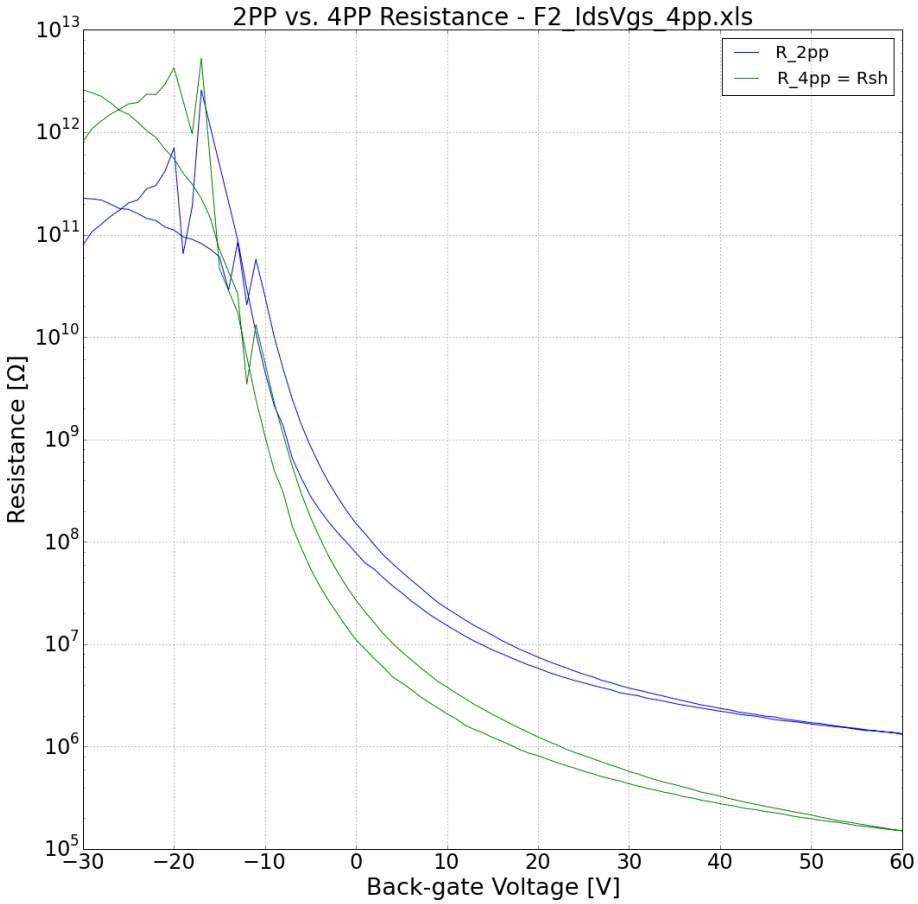

Fig. 10 Example 4PP (sheet resistance) and 2PP resistances measured for the example device data in Fig. 9

As expected, the resistance drops as the gate voltage increases, a result of the accumulation of more electrons. At roughly –15 V, the MoS_2 channel is depleted and shows a very high resistance. The sheet resistance at a gate voltage of +60 V was recorded for every device and is used for a comparison in Section 3.2.

2.3.4 Contact Resistance and Transfer Length Extraction

The contact resistance was estimated[12,13] by comparing the measured 4PP and 2PP resistances:

$$2R_c = R_{2PP} - R_{4PP}\frac{\frac{L}{W_{2PP}}}{\frac{L}{W_{4PP}}} \quad [\Omega]. \tag{2}$$

The contact resistance at a back-gate voltage of +60 V for every device is compared in Section 3.3. Since the measured contact resistance is geometry dependent, the contact resistance is often normalized by the contact width to become R_cW [Ω·μm] or the contact area to become the contact resistivity, $\rho_c = R_c \cdot Area_{contact}$ [Ω·μm^2]. In these devices, the contact width is 1 μm and the contact area is 0.5 μm^2. Plotted in Fig. 11 are the normalized contact resistances.

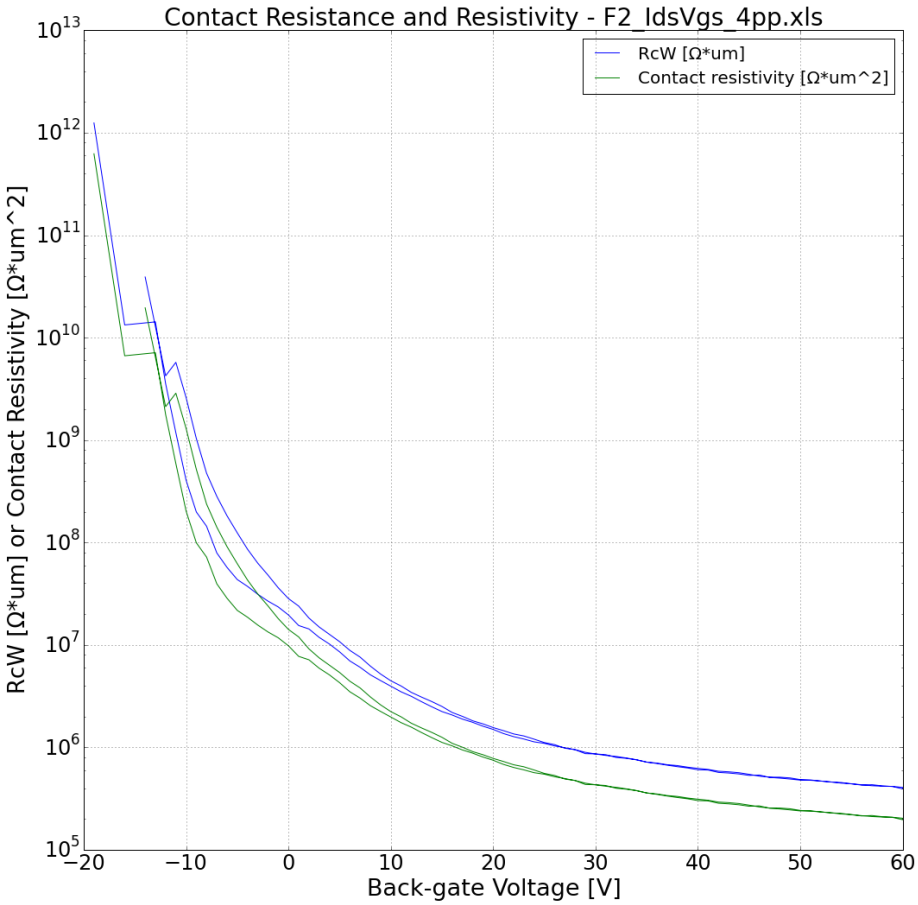

Fig. 11 Example contact resistivity measured for a single device. The green curve is normalized by the contact width and the blue curve by the contact area. The contact resistance shows a significant dependence on the gate voltage.

To further characterize the contacts, the transfer length is calculated as the square root of the ratio of the contact resistivity over the sheet resistance:

$$`L_T = \sqrt{\frac{\rho_c}{R_{sh}}} = \sqrt{\frac{R_c A_c}{R_{sh}}}. \tag{3}$$

Ideally, the transfer length is very small because the contact resistance is significantly less than the sheet resistance. If the transfer length is less than the length of the contact, then the contact resistivity can be recalculated as $\rho_c = R_c \cdot L_T W$ [Ω·μm^2]. Figure 12 displays the measured contact resistivity, sheet resistance, and transfer length for the example device data. The transfer length was consistently around 1 μm, meaning these contacts are not efficiently injecting current.

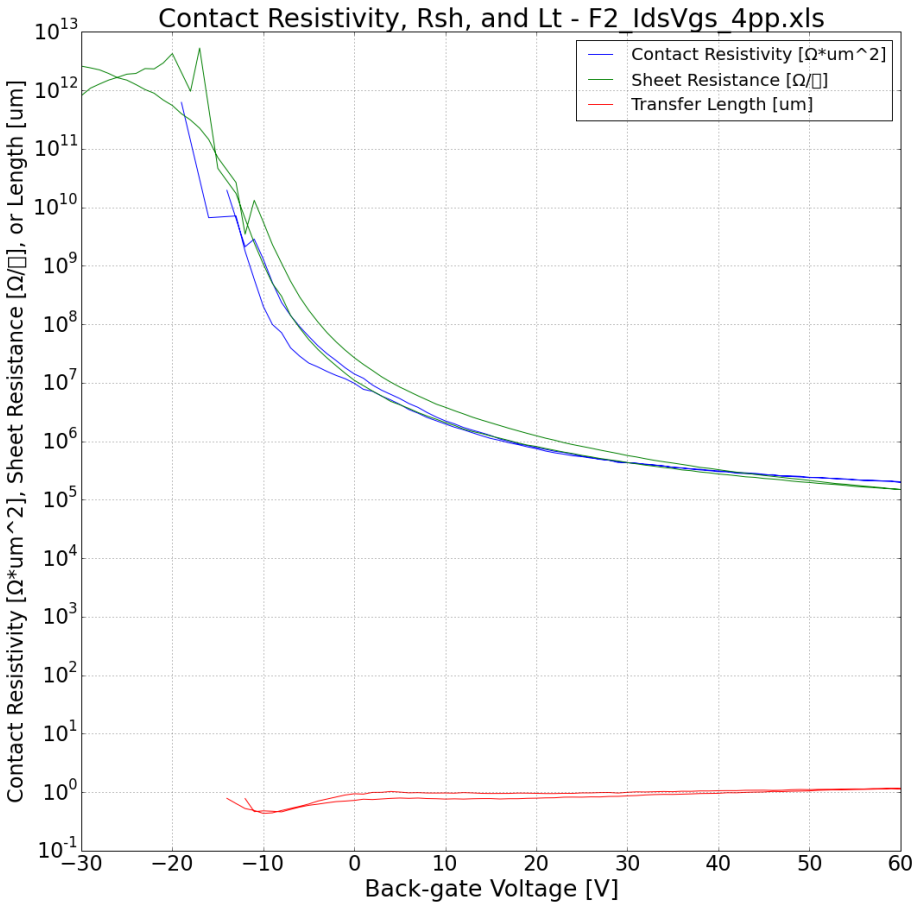

Fig. 12 Example contact resistivity, sheet resistance, and transfer length measured for a single device

In general, the transfer length was found to increase slightly with gate voltage; however, a few devices showed a slight decrease. Both the sheet resistance and contact resistance continually decrease with gate voltage, meaning that the sheet resistance decreases faster than the contact resistance.

2.3.5 Threshold Voltage Extraction

To extract the threshold voltage, the extrapolation in the linear region method[14] was used. As shown in Fig. 13, this method consists of determining the maximum slope

of the current with respect to the gate voltage and extrapolating the x-intercept, which represents the threshold voltage. Since the sweeps in both directions do not have identical measured results (hysteresis is present), the data were split based on the sweep direction for analysis purposes. To accurately determine the slope of the current at any gate voltage, the data were first smoothed. A spline was fitted to the raw data to smooth the data and allow differentiation.

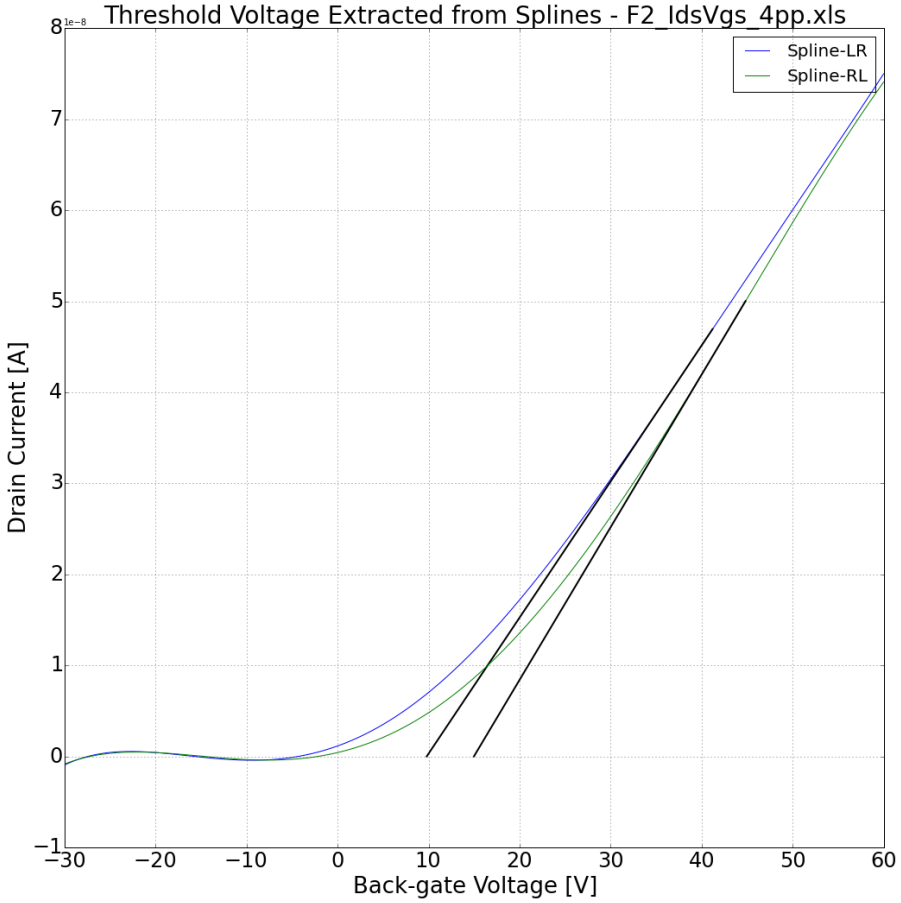

Fig. 13 Example of threshold voltage extraction using splines to fit the drain current. A threshold voltage of roughly 10 and 15 V is extracted for the left-to-right (LR) and right-to-left (RL) sweeps, respectively.

Figure 14 shows the maximum slope extracted from the splines, plotted against the original data to demonstrate the spline method's accuracy.

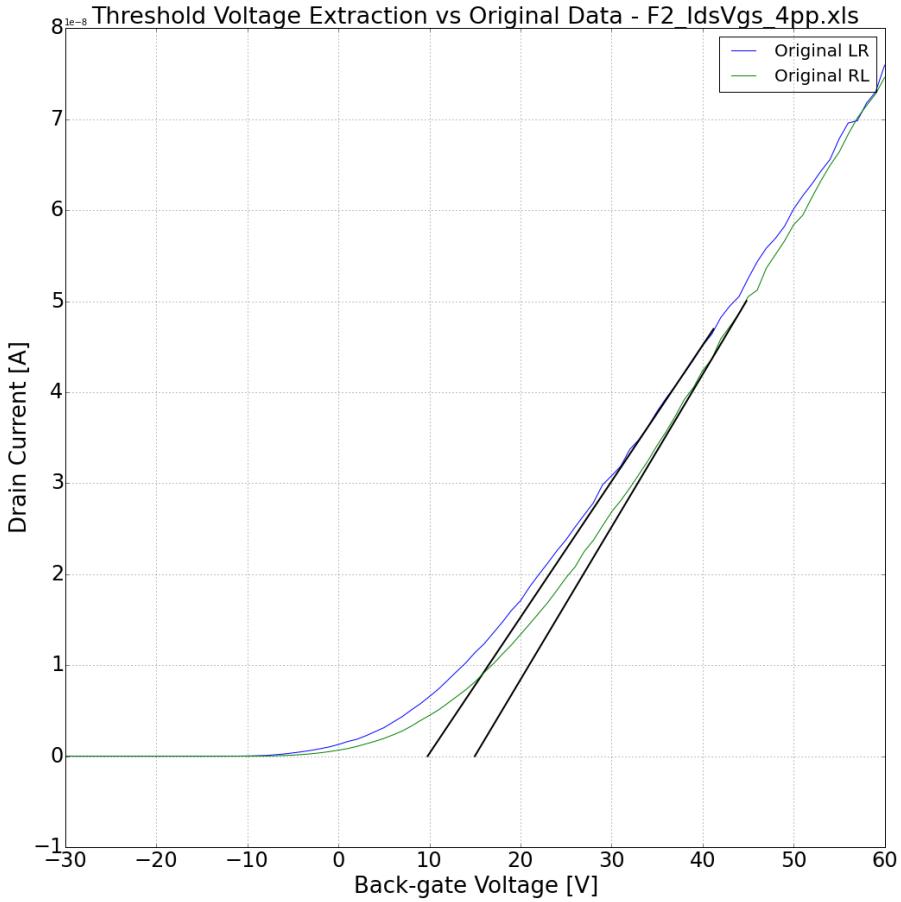

Fig. 14 Threshold voltage extracted from the maximum slope of the splines, plotted along with the original drain current data

Determining the maximum slope from the jagged original data would lead to spurious threshold values, but we can see here that the results of the splines fit the original data well.

A second method, based on the measured conductance between the inner 2 probes, $G_{4PP} = {R_{4PP}}^{-1} = I_{ds}/V_{diff}$, was also used to calculate the threshold voltage. The motivation for using a second method was to decouple the impact that the contact resistance and the MoS_2 channel have on the threshold voltage. The measured current is impacted by the parasitic contact resistance, but ideally the measured 4PP conductance should not be impacted. Additionally, the measured 4PP conductance was usually smoother and more consistent than the measured drain current. Figure 15 shows the measured 4PP conductance for our example device data as well as the spline fitting.

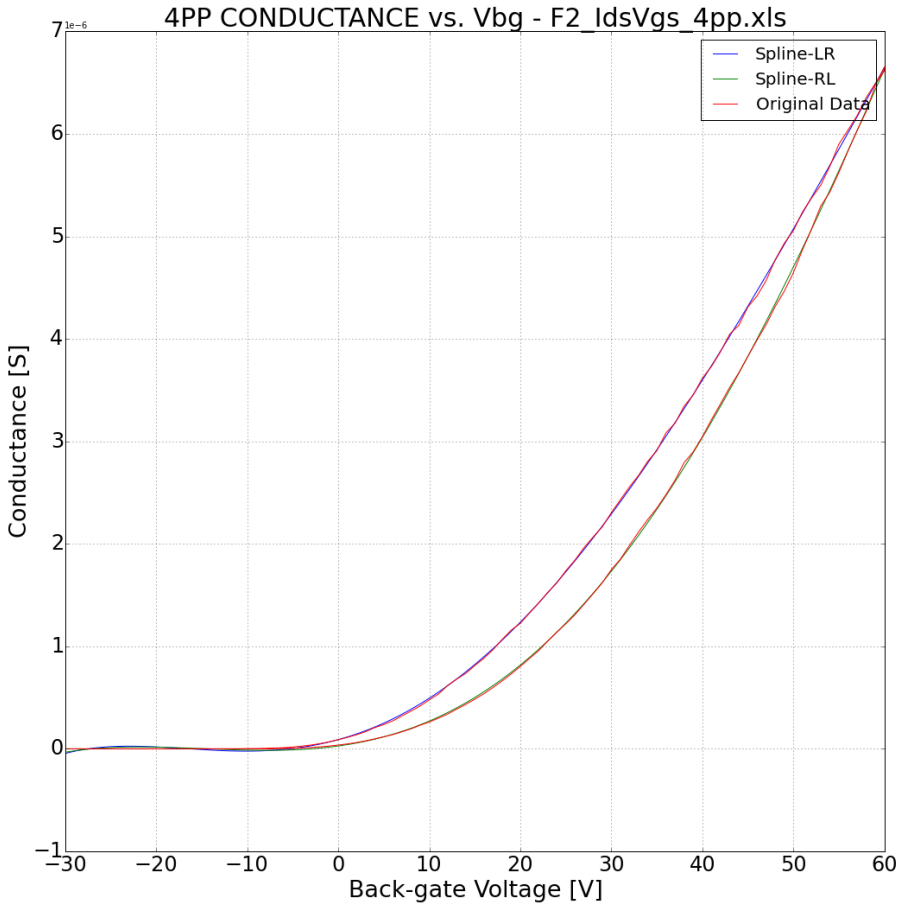

Fig. 15 Measured 4PP conductance of the example device data and the fitted splines for each direction

Just as in the previous method based on the current, the maximum slope of the conductance splines are determined for each sweep direction as well as the x-intercept. Shown in Fig. 16 are the maximum slopes plotted along with the original data.

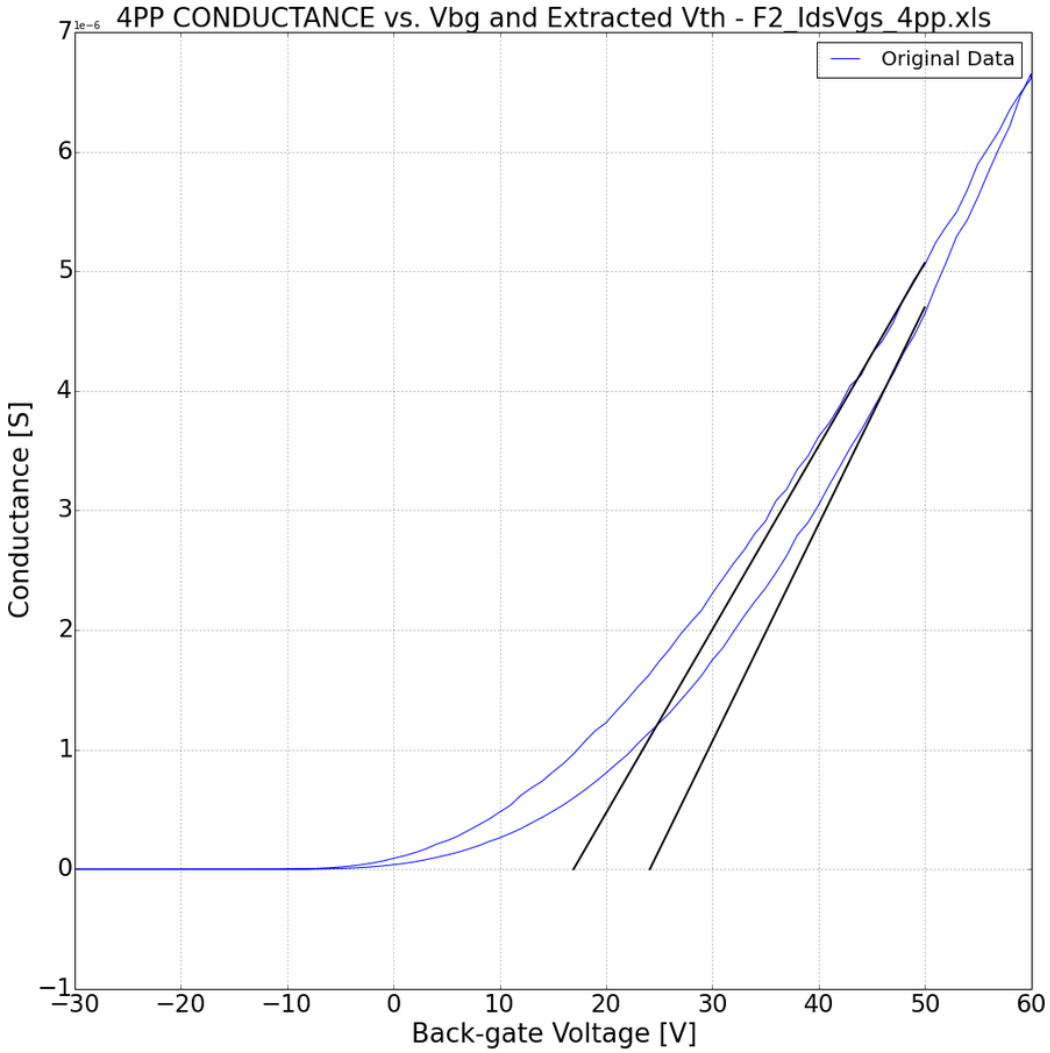

Fig. 16 Example threshold voltage extraction, comparing the maximum slope of the splines to the original 4PP conductance. A threshold voltage of roughly 17 and 24 V is extracted for the LR and RL sweeps, respectively.

2.3.6 Hysteresis Extraction

For this experiment, hysteresis was calculated as the difference in extracted threshold voltages for the 2 sweep directions of the back-gate voltage. For example, the hysteresis for the data shown in Fig. 16 would be 24 V – 17 V = 7 V. Since 2 methods were used to extract the threshold voltage, 2 values of hysteresis are calculated for every device (i.e., a hysteresis related to the drain current and a hysteresis related to the 4PP conductance). It should be noted that the sweeping speed of the back-gate voltage will impact the amount of hysteresis measured. The sweep speed used in these measurements averaged 1.7 V/s. The range of applied back-gate voltages will also affect the amount of hysteresis measured, and the back-gate voltage range of –30 to + 60 V was kept constant for every device.

2.3.7 Field-Effect Mobility Extraction

Carrier mobility reflects the ease at which an electron or hole can travel through a material. Often the field-effect mobility is extracted from a transfer curve using the following equation[3,15]:

$$\mu_{FE\ \ 4PP} = \frac{d\frac{I_{ds}}{V_{diff}}}{dV_{bg}} \times \frac{1}{C_{gate}} \times \frac{L}{W_{4PP}} \quad [\mathrm{cm^2/V{\cdot}s}], \tag{4}$$

where C_{gate} is the capacitance coupling per unit area between the degenerately doped Si and the MoS_2 monolayer. The SiO_2 layer for these devices is 220 nm thick, creating a capacitance per area of 1.57×10^{-4} [F/m^2], assuming a relative permittivity, $\varepsilon_{r\ SiO2}$, of 3.9. Figure 17 plots the result of applying Eq. 4 to the example device data from Fig. 9. As was the case with the threshold voltage, a value for the mobility was calculated for each sweep direction of the back-gate. The mobility extracted for both directions was then averaged and the maximum value of the average mobility is reported. Smooth differentiation was achieved using the same spline method as introduced in Section 2.3.5.

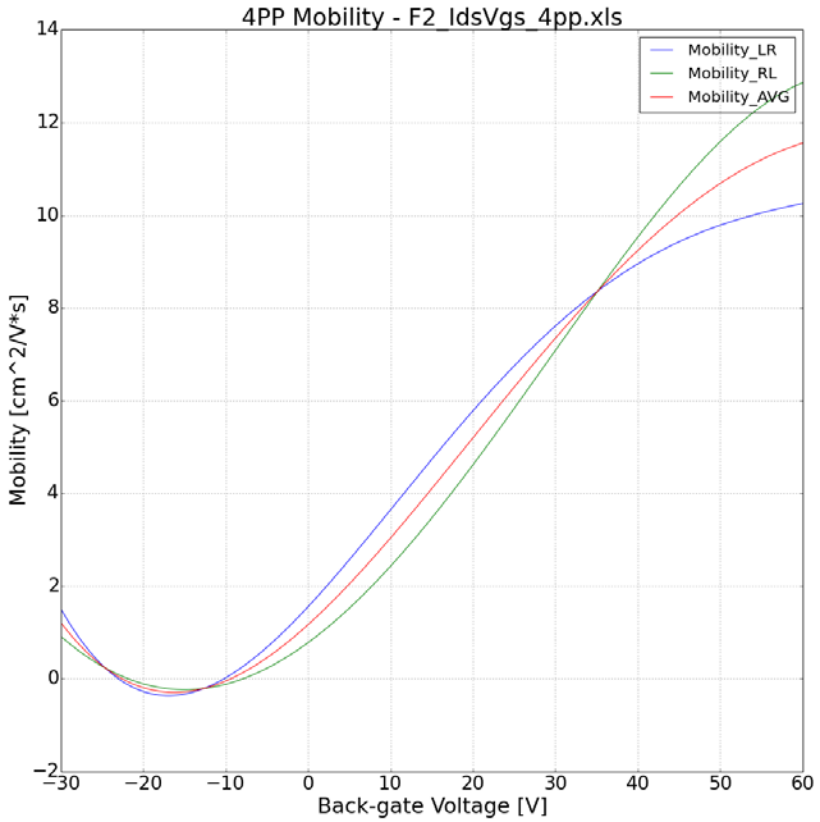

Fig. 17 Example field-effect mobility extracted for the example device, showing both sweep directions of the back-gate and their average. Note that the mobility shown on the negative gate voltage side is inaccurate and is an artifact as a result of the splines not fitting the flat line of approximately 0 conductance well (see Fig. 15).

3. Results and Discussions

3.1 Maximum Current

The maximum current measured (at V_{bg} = +60 V) for every device tested is plotted in Fig. 18. This simple metric is inversely related to the contact resistance at the MoS_2-metal interface and the sheet resistance of the MoS_2. Samples 103A and 198A have comparatively lower currents, which means their contact resistance, sheet resistance, or both are significantly higher than the other samples.

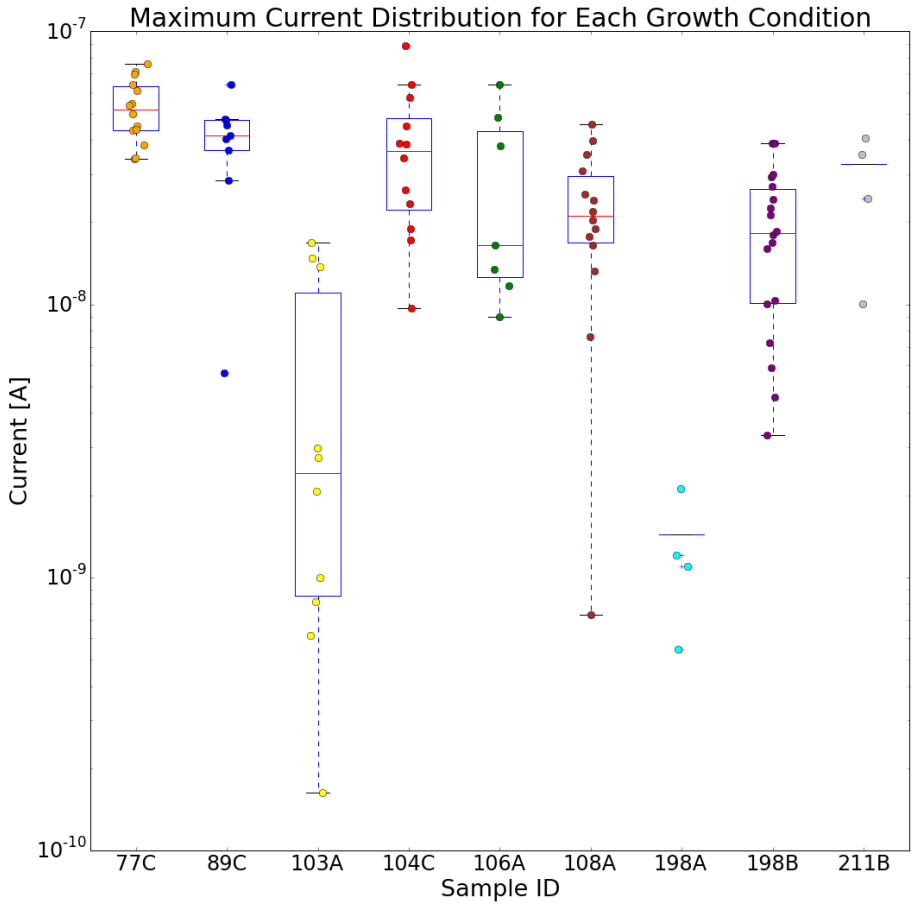

Fig. 18 Boxplot displaying the maximum measured current in every device, separated by sample ID (growth condition)

Sample 103A was grown using the same growth conditions as 77C, and 198A had the same growth conditions as 198B, but was transferred to a new SiO_2 substrate. The other 7 samples consistently had maximum currents in the 10- to 100-nA range.

3.2 Sheet Resistance

The sheet resistance of each device at a gate voltage of +60 V is plotted in Fig. 19. The sheet resistance was measured in the 4PP configuration, giving an "intrinsic" characterization of the MoS_2 material by excluding the contact resistance. Samples 103A and 198A do not show a high sheet resistance, hinting that the reason for their limited current flow is due to high contact resistance.

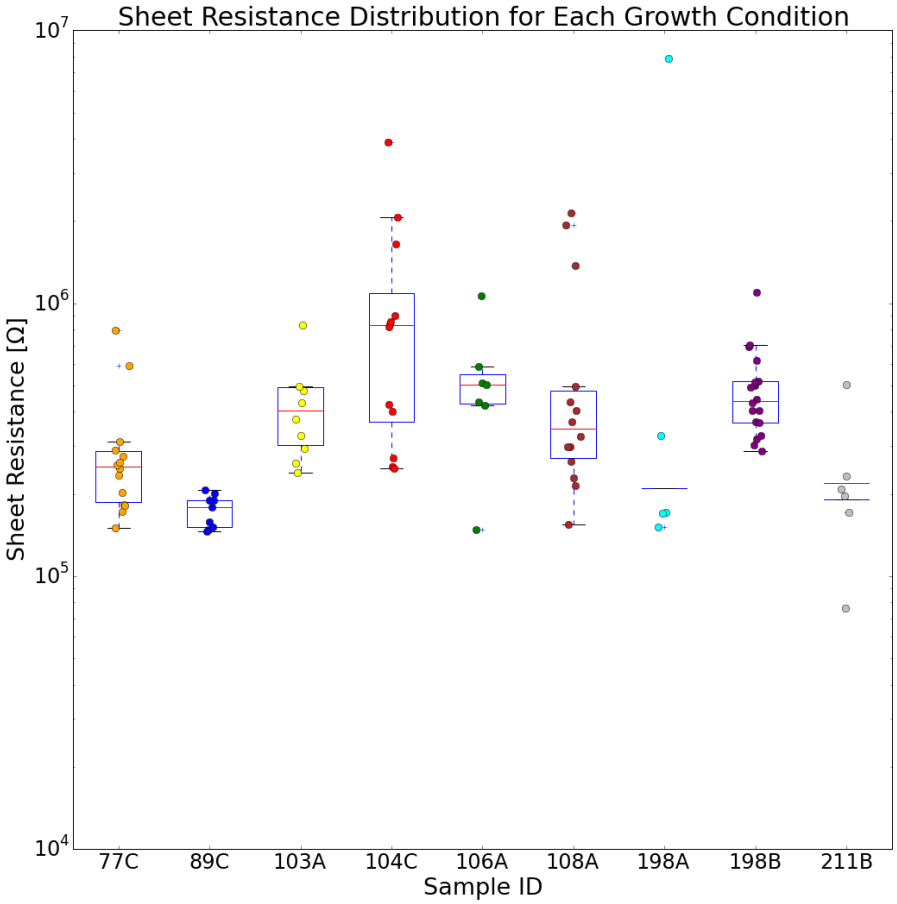

Fig. 19 Boxplot displaying the measured sheet resistance in every device at a back-gate voltage of +60 V, categorized by sample ID (growth condition)

Sample 89C has both the lowest and most consistent sheet resistance. 89C had a growth time of 50 min, compared to 10 min for every other. The longer growth time could create a less defective crystal by healing defects with more time and energy to rearrange atoms into a more ideal crystal. Sample 104C shows the largest range and highest average sheet resistance. It should be noted that 104C was grown with a lower purity sulfur precursor, which could be creating a more defective crystal and this higher sheet resistance. To confirm this, transmission electron microscopy is needed to determine the crystalline quality of each sample and X-ray photoelectron spectroscopy to compare the S-to-Mo ratio.

3.3 Contact Resistance and Transfer Length

The contact resistance was measured for each device at a back-gate voltage of +60 V and is plotted in Fig. 20.

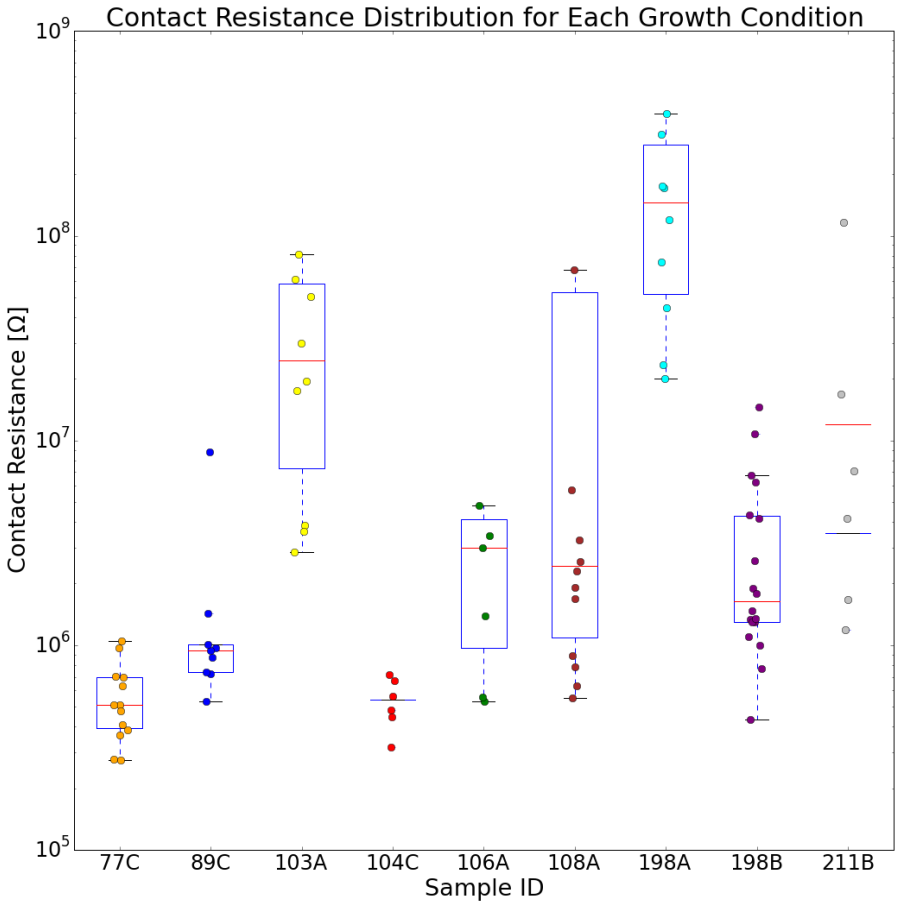

Fig. 20 Boxplot displaying the contact resistance measured for every device at V_{bg} = 60 V, separated by sample ID (growth condition)

The transferred sample, 198A, had the highest average contact resistance. Residue from the transfer process could potentially explain the increase in contact resistance for this sample.

Sample 103A also had comparatively high contact resistance. 103A was grown with the same growth conditions as 77C and should ideally have similar contact resistance. One possible reason for the discrepancy could be that both 198A and 103A were part of the second batch of devices, which had a shorter anneal time before testing in the probe station. If this were the reason, one would expect 211B to have high contact resistance as well, since it was also in the second batch. 211B does have a high average contact resistance, but it is very inconsistent and inconclusive.

In general, the 2PP properties are difficult to use to draw conclusions about the material quality due to the inconsistent, gate-dependent, and large contact resistance. Therefore, metrics extracted from the 4PP measurements are more reliable to examine trends in the electrical properties. Looking back at Fig. 19, the sheet resistance of sample 77C and 103A is very similar.

Regardless of the growth condition used, the contact resistance measured is sometimes orders of magnitude higher than usual device requirements such as R_c accounting for at most 20% of the total device resistance.[16] However, this agrees with some results in the literature of high contact resistance seen for Ti contacts to monolayer MoS_2.[13]

The transfer lengths (plotted in Fig. 21) averaging over 1 μm further confirms the inefficiency of current injection since the transfer length is longer than the contact length.

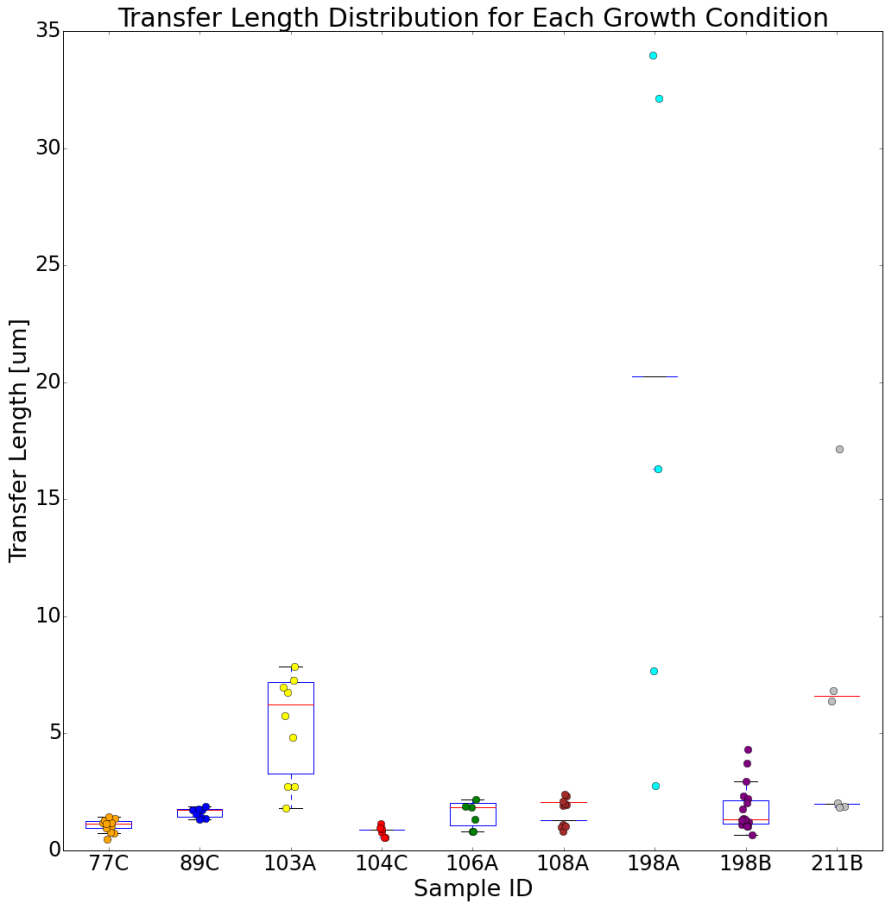

Fig. 21 Boxplot displaying the transfer length measured in every device at V_{bg} = 60 V, separated by sample ID (growth condition)

3.4 Threshold Voltage

The threshold voltage measured for every device using the extrapolation in the linear region of the drain current is plotted in Fig. 22.

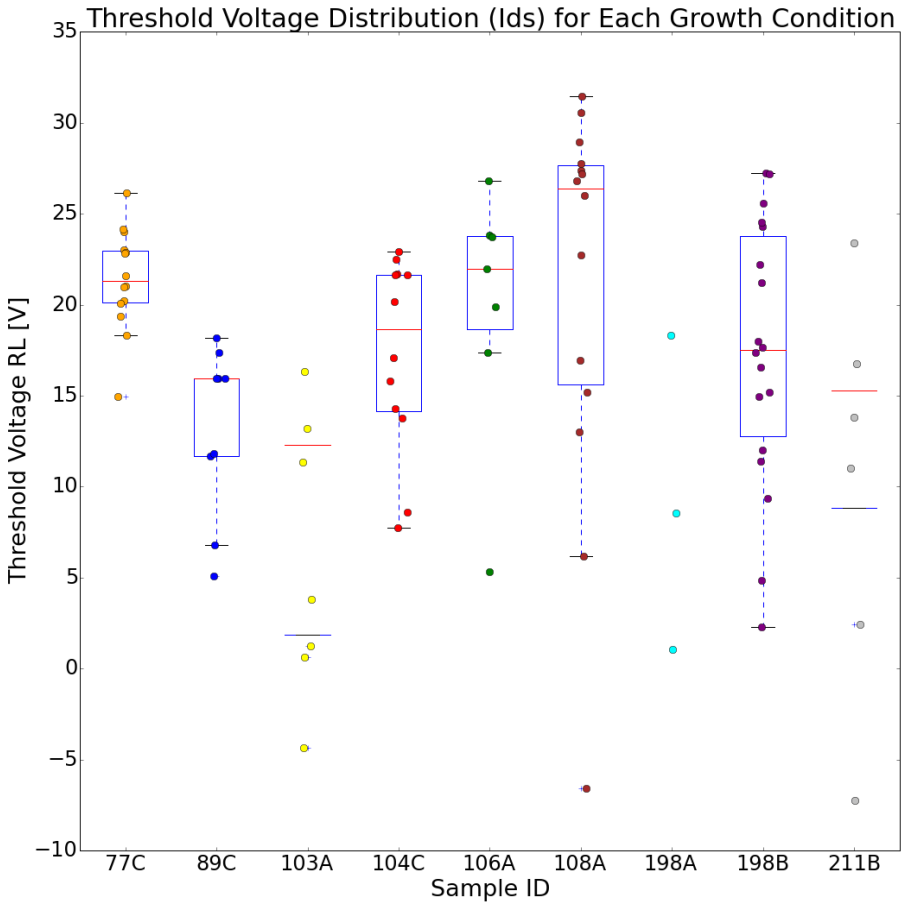

Fig. 22 Extracted threshold voltage for every device, using the maximum slope of the current. The threshold voltage plotted here was calculated using the sweep of the gate voltage from +60 to –30 V (i.e., RL).

As discussed in Section 2.3.5, the threshold voltage extracted with this method is affected by the contact resistance. The contact resistance in these MoS_2 transistors is known to be extremely high and gate-dependent, which leads to an inconsistent threshold voltage.

On the other hand, using the second method discussed in Section 2.3.5 based on the 4PP conductance, a more consistent picture of the threshold voltages is achieved. The threshold voltage measured for every device, using the extrapolation in the linear region of the 4PP conductance is plotted in Fig. 23.

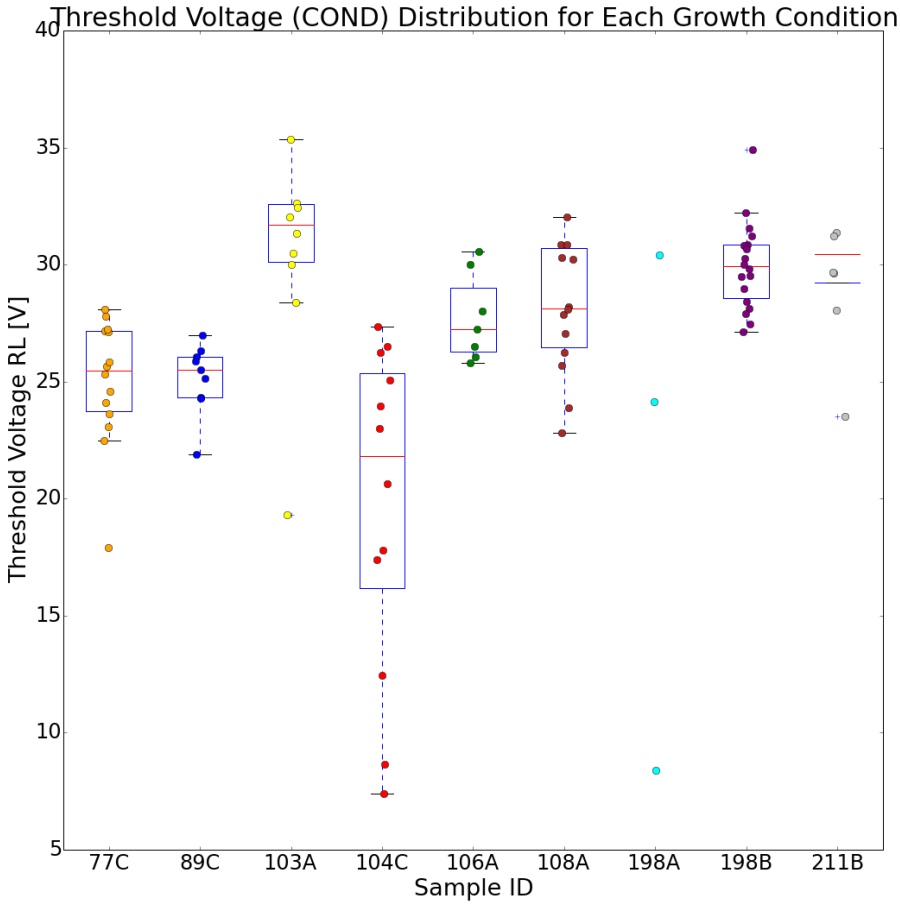

Fig. 23 Extracted threshold voltage for every device using the maximum slope of the 4PP conductance. The threshold voltage plotted here was calculated using the sweep of the gate voltage from +60 to –30 V (i.e., RL).

The extracted threshold voltage is between 22.5 and 32.5 V for nearly every device, except for the devices of sample 104C, which was grown with a lower quality sulfur powder precursor. This observation implies that using a lower purity sulfur leads to a more inconsistent, more negative threshold voltage. Previous studies have linked sulfur vacancies to a negative shift in threshold voltage.[17] In this case, defect states are created within the MoS_2 bandgap that enable more current flow during the subthreshold regime. Similar defect states due to sulfur vacancies or impurities could be responsible for the observed behavior of sample 104C.

3.5 Hysteresis

Hysteresis in MoS_2 transistors is thought to arise from interface traps between the MoS_2 and SiO_2 substrate,[18] the interaction with atmospheric adsorbates,[19] and an intrinsic property to the MoS_2 material.[20,21]

The hysteresis was measured for each device as the difference between threshold voltages for each gate sweep direction. Since 2 methods were used to extract threshold voltage, 2 values of hysteresis are calculated. Using the first method, based on the maximum slope of the current, the hysteresis measured for every device is plotted in Fig. 24.

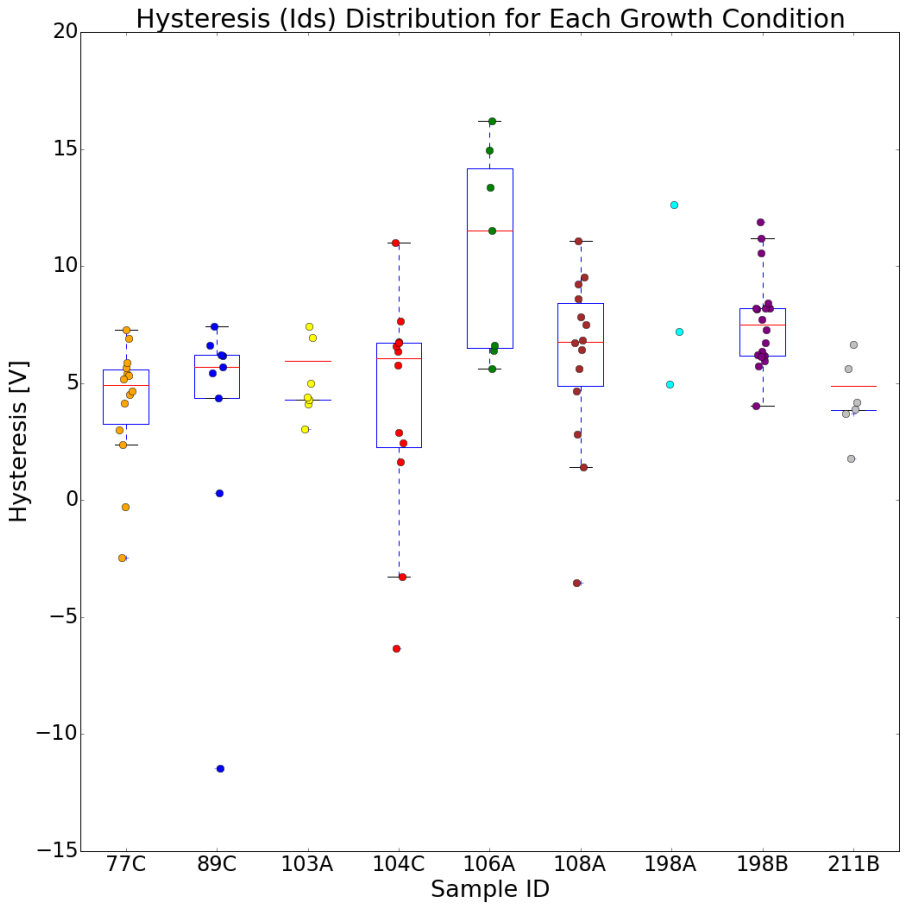

Fig. 24 Extracted hysteresis for every device, calculated as the difference in threshold voltages measured via the maximum slope of the current method described in Section 2.3.5

Using the second method, based on the maximum slope of the 4PP conductance, the hysteresis measured for every device is plotted in Fig. 25.

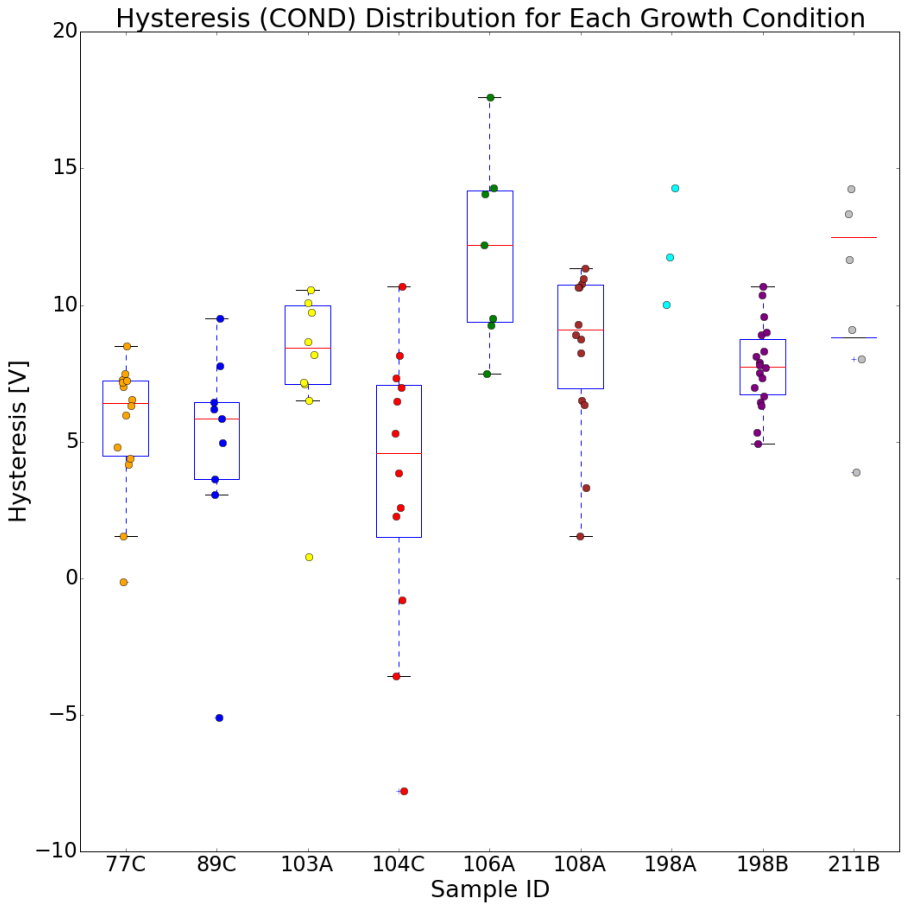

Fig. 25 Extracted hysteresis for each device, calculated as the difference in threshold voltages measured via the maximum slope of the 4PP conductance method described in Section 2.3.5

Even with testing in vacuum and vacuum annealing at 400 K beforehand, all growth conditions led to transistors with significant hysteresis. Sample 106A had the highest measured hysteresis, regardless of the method used to quantify it. This sample was grown with a lower sulfur heating tape temperature, which would decrease the amount of sulfur present for reaction at the substrates, possibly resulting in sulfur vacancies or different edge terminations that could increase the amount of charge trapping. Sample 104C (low purity sulfur) had a very inconsistent hysteresis, similar to its inconsistent threshold voltage.

3.6 Field-Effect Mobility

The maximum field-effect mobility for each device is plotted below in Fig. 26. The highest average mobility was seen in sample 89C, the 50-min growth sample. A longer growth time could improve the crystalline quality of the MoS_2 by healing defects that are present in the samples with a shorter growth time.

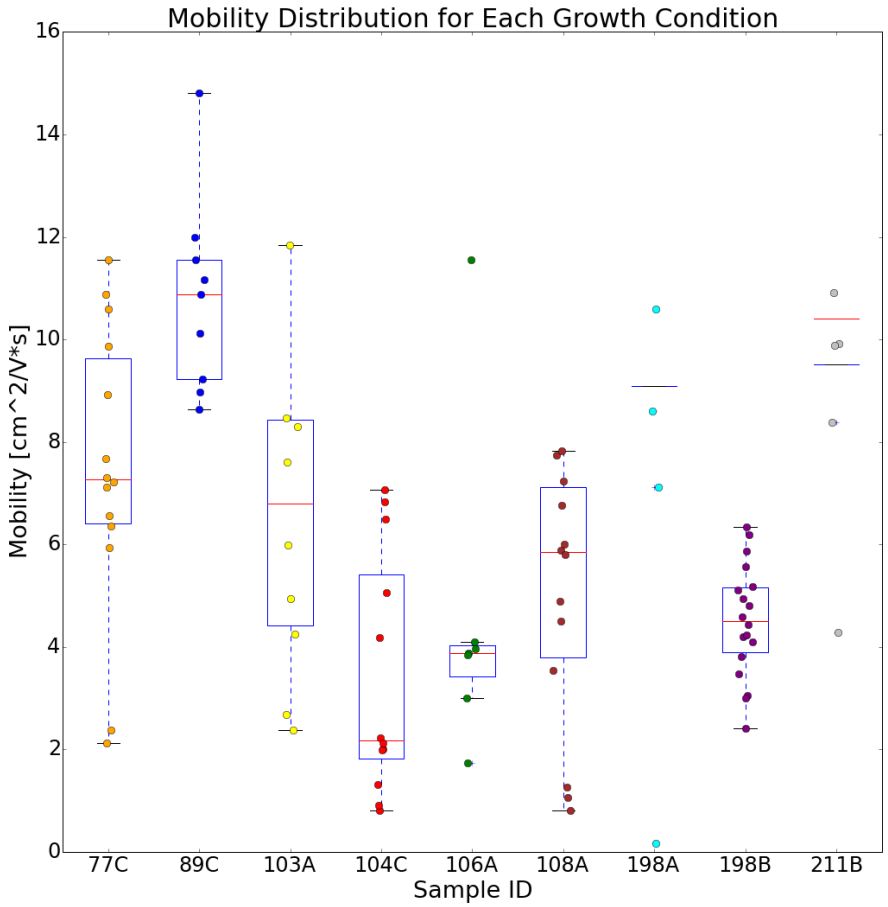

Fig. 26 Boxplot displaying the maximum mobility measured in every device separated by sample ID (growth condition)

The 2 samples with the lowest average mobility were grown with low-purity sulfur (104C) and at a lower sulfur temperature (106A). Samples 77C and 103A had the same growth condition and show similar average mobility; however, there is a large range in recorded values.

The mobility values reported in the literature for monolayer PV or CVD MoS_2 on SiO_2[22] agree well with the values obtained in this study (1–15 $cm^2/V \cdot s$).

Sample 198A had many devices where the data were inconsistent at high gate voltages, preventing an accurate mobility from being extracted. For the devices on 198A that did work, their mobility values were higher than any measured devices on sample 198B (which was the same growth, but without transferring). This implies that transferring can be beneficial in terms of improving the mobility; however, the transfer technique needs to be improved to make it a consistent improvement.

Sample 211B had a low yield for reasons related to the growth; larger triangles formed primarily around the edges of the substrate, limiting the number of device locations. Interestingly, for the devices that did work, the extracted mobility for 198A and 211B was close to that of sample 89C.

The extracted mobility likely increased with higher gate voltage (see Fig. 17) due to the screening of charged impurities with increasing carrier density.

Ma and Jena[23] argue that most current MoS_2 devices are limited by charged impurity scattering and that only after reducing impurities below a level that is dependent on the dielectric environment will scattering from remote optical phonons determine the upper limit on achievable mobility. Comparing our extracted mobility with their findings, it appears the mobility in these devices is limited by charged impurity scattering. Ma and Jena determined a relationship between mobility, carrier density, impurity density, and the dielectric environment. Using our measured mobility at +60 V_{bg} and carrier density (usually around 3.5×10^{12} cm^{-2}, estimated as $n = (C_{gate}/q)(V_{bg}-V_t)$, where q is the elementary charge value) as inputs to their model, the average impurity density in our MoS_2 is approximately 1 to 3×10^{13} cm^{-2}.

For MoS_2 devices with high impurity levels (10^{13} cm^{-2}), a high-κ dielectric can improve mobility through dielectric screening. However, high-κ dielectrics also have lower energy phonon modes, which leads to an increase in remote optical phonon scattering. Based on the calculations by Ma and Jena, a greater mobility improvement is achieved by lowering the impurity concentration and using low- κ, high-energy phonon mode dielectrics. Therefore, while a high-κ dielectric may improve our current device performance, it is also important to modify the growth or fabrication process to limit the impurity concentrations and improve mobility.

3.7 Fabrication Yield

At least 10 transistors were desired on each growth condition to provide statistics on device performance. Unfortunately, samples 198A and 211B only provided a few working devices. Devices on 198A suffered from extremely high contact resistance and scattering, which we attribute to issues with the KOH transfer or fabrication process. Sample 211B used an alternate boat configuration, which resulted in large triangles toward the edges of the sample, making fabrication difficult and ultimately limiting the number of devices made. We are in the process of improving the MoS_2 coverage for this setup.

4. Conclusions

MoS_2 was grown on SiO_2 substrates using different growth conditions and multiple identical transistors were fabricated for each growth condition using MoS_2 as the channel material. Every transistor was characterized electrically to provide statistics on metrics such as sheet resistance, electron mobility, threshold voltage, hysteresis, and contact resistance.

The performance of the MoS_2 was found to vary significantly between growth conditions, though inconsistencies were noticed within the same growth condition or sample. Reproducibility issues are likely due to the difficulty of controlling the local growth environment when working with solid sources.

The contact resistance for Ti contacts to MoS_2 was very poor. The impact of evaporation pressure on the contact quality for Ti has been studied[24] and could possibly be applicable to our devices. Other groups have had success using alternative metal contacts such as silver,[25] and we are in the process of investigating other metals ourselves.

Since the contact resistance was found to be very large, conclusions on the electrical data are mainly drawn from the sheet resistance, threshold voltage, hysteresis, and field-effect mobility, which can all be measured in a 4PP configuration.

Growing for a longer period of time improved transistor performance, as indicated by the performance of sample 89C, which underwent a 50-min growth process as opposed to 10 min for every other sample. 89C had the highest average electron field-effect mobility (11 $cm^2/V \cdot s$) and the lowest and most consistent sheet resistance. Consistency in the threshold voltage and hysteresis was also evident, though other growth conditions performed as well.

Growing with the 2-boat setup (sample 211B) yielded very few devices due to the growth being concentrated on the edges of the sample. However, for the few devices tested, the electron mobility extracted was similar to that of the best performing sample (89C), prompting this growth setup to be investigated more in detail. A similar situation occurred for the transferred sample (198A), where the device yield is low due to potential transfer issues; however, the devices that were measurable gave mobility values higher than the sample that was not transferred (198B). This higher performance post-transfer supports the idea of removing strain or interfacial impurities to improve device performance[8], but the limited device yield suggests improvements need to be made to the transfer process including the possibility of switching to a resist-free[9] transfer process.

Using a lower purity sulfur precursor resulted in degraded transistor performance, suggesting precursor quality plays an important role in the electrical properties of MoS_2. The sample grown with lower purity sulfur (104C) had the lowest carrier mobility and highest sheet resistance, suggesting a more defective crystal with more scattering centers. Sample 104C also had the most negative threshold voltage when using the intrinsic conductance method and the most inconsistent hysteresis values measured. Interestingly, the contact resistance measured on sample 104C tied for the lowest measured, hinting that creating a defective contact area may reduce contact resistance. This idea has been pursued by a few research groups already.[26,27]

Lowering the sulfur temperature also degraded transistor performance. Sample 106A was grown with a lower sulfur heating tape temperature (200 °C instead of 250 °C) and had the highest measured hysteresis, the second lowest electron mobility, and second highest sheet resistance. Lowering the temperature of the sulfur heating tape decreases the amount of sulfur available for reaction at the surface of the substrate, which could manifest as sulfur vacancies or different edge terminations.

Lowering the temperature of the furnace from 700 to 650 °C (sample 108A) did not improve any performance metric, but also did not substantially degrade any either. Decreasing the sulfur temperature or changing sulfur purity was more significant than lowering the furnace temperature.

Going forward, we hope to investigate the 2-boat process more, characterize growth on quartz and sapphire substrates, and attempt to improve processing steps such as the transfer and metal contact.

5. References

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Appendix. Impact of Light on Electrical Measurements

One device per growth substrate was tested first with the aluminum foil blocking the light and again with the sample illuminated by white light. All tests showed light sensitivity, though with varying magnitude, highlighting the importance of measuring in the dark. Figure A-1 shows the impact of light measured on sample 104C.

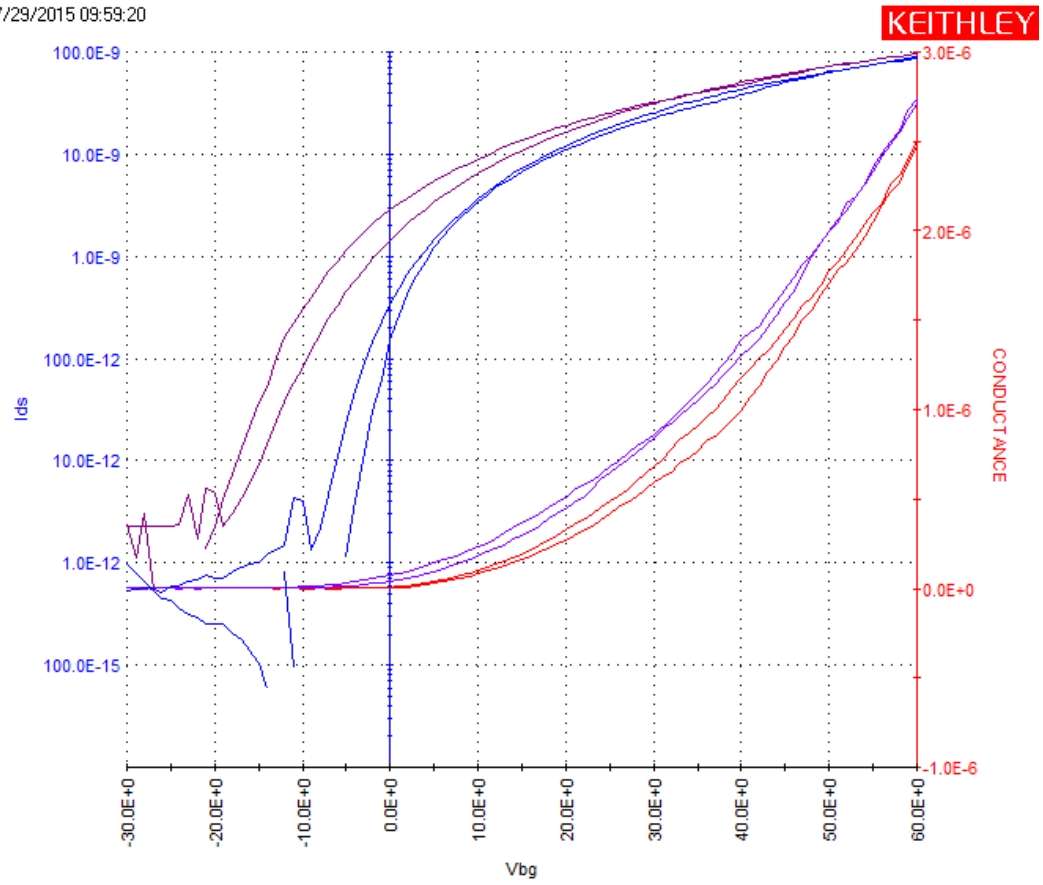

Fig. A-1 Drain-source current and 4-point probe (4PP) conductance measured on sample 104C in both a dark and illuminated condition. Upon illumination, both the current and conductance increase. The conductance measured in the dark is drawn in red, the illuminated conductance is plotted in purple. The current measured in the dark is plotted in blue, the illuminated current is plotted in purple.

List of Symbols, Abbreviations, and Acronyms

2-D	two-dimensional
4PP	4-point probe
ARL	US Army Research Laboratory
Au	gold
CF_4	tetrafluoromethane
CVD	chemical vapor deposition
DI	deionized
EBL	electron beam lithography
FET	field-effect transistor
H_2O_2	hydrogen peroxide
H_2SO_4	sulfuric acid
IPA	isopropyl alcohol
KOH	potassium hydroxide
LR	left-to-right
MIBK	methyl isobutyl ketone
MoO_3	molybdenum trioxide
MoO_xS_y	molybdenum oxysulfide
MoS_2	molybdenum disulfide
N_2	nitrogen gas
O_2	oxygen
PMMA	poly(methyl methacrylate)
PTAS	perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt
PV	powder vaporization
RF	radio frequency
RIE	reactive ion etching

RL	right-to-left
S	sulfur
Si	silicon
SiO_2	silicon dioxide
Ti	titanium

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